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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,550	07/24/2003	Young-Woo Kim	053933-5051	8213

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EXAMINER	
LEPISTO, RYAN A	

ART UNIT	PAPER NUMBER
2883	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,550	KIM ET AL.	
	Examiner	Art Unit	
	Ryan Lepisto	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. **Claim 5** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Lines 9 and 11 both claim a first step; only one of the steps can be performed first. If both are to be done at the same time, the claim should make that clear. For this action, the office will assume the step of layering the patterned copper clad laminates on each other is done first, followed by drilling electric and optic via holes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-3, 5, 8-10 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of **Booth et al (US 5,386,627)** (Booth) and **Tsukamoto et al (US 6,438,281 B1)** (Tsukamoto).

Booth teaches a method of fabricating a multi-layered integrated circuit (Fig. 2) with via holes. Booth teaches forming a plurality of via holes (120) through copper

circuit patters (102) that are adhered to a di-electric insulating layer (100) using a drill (either a CO_2 laser beam or mechanical drill) (column 3 lines 44-47), plating the inner wall of each via hole (120) (column 3 lines 65-66), exposing and etching the plated portion (102) of an upper (104) and lower (106) side of the integrated circuit to form a circuit pattern on the upper and lower sides (column 3 lines 17-34) and layering the integrated circuits (150) on each other using an insulating resin adhesive (140) (column 3 lines 51-60 and Fig. 2).

The structure created by the process taught by Booth creates a printed circuit board (Fig. 2) comprising a plurality (each layer 150 has the same structure) of copper clad layers (102), copper plated via holes (120) that are devoid of insulating resin, and a circuit pattern on the upper (104) and lower (106) side of each integrated circuit (150), an insulating resin (140) used to layer the interposing layers (150).

Booth does not teach expressly removing the insulating resin adhesive (140) from the via holes, but since the insulating resin adhesive (140) does not fill the entire via (120) it does not need to be removed to create the via.

Booth also does not teach expressly a second drilling step to create more vias, but since the Booth reference does drill via holes it does not destroy the reference if one via hole is drilled after the step shown in Fig. 1A. and other is formed after the step shown in Fig. 1B. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with one drilling step because via holes are still created.

Booth also does not teach expressly opto-via holes or an optical waveguide positioned to propagate an optical signal.

Tsukamoto teaches an optoelectric wiring substrate comprising both electrical traces and optic via holes and the method of making the same. Tsukamoto teaches copper laminate layers (Fig. 5, 531) (column 11 lines 9-14), etching layers to form circuit traces (column 11 lines 30-35), attaching a copper wiring layer (51) to a substrate using an adhesive (column 9 lines 51-55) and contains electrical-optical via holes (523, 545) and a waveguide (501) to propagate an optical signal.

Booth and Tsukamoto are analogous art because they are from the same field of endeavor, processes to create integrated circuit and via holes.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a waveguide in the interposing layers (150) as taught by Booth like the waveguide taught by Tsukamoto and to use the existing via holes as taught by Booth to propagate a signal from a waveguide since the via holes are capable of propagating light.

The motivation for doing so would have been increase speed and efficiency of the system by replacing some electric wiring with optical wiring to that optical signals so not to create noise or electromagnetic waves (Tsukamoto, column 1 lines 44-49).

3. **Claims 4, 7, 11 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Booth and Tsukamoto as applied to claims 1-3, 5, 8-10 and 12 above, and further in view of **Endoh et al (US 5,502,893)** (Endoh).

The combination of Booth and Tsukamoto teaches the integrated circuit with the limitation described above used to reject claims1-3, 5, 8-10 and 12 above.

The combination of Booth and Tsukamoto does not teach expressly an epoxy resin with 95% or more light transmissivity filled in the optical via holes.

Endoh teaches method of creating via holes comprising the step of filling the holes with an epoxy resin (5), prepreg (column 3 lines 14-17), that is the same as the preferred resin disclosed by the applicant (specification, page 11 lines 17-18).

The combination of Booth and Tsukamoto and Endoh are analogous art because they are from the same field of endeavor, processes to create integrated circuit and via holes.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to substitute the resin as taught by Booth to the prepreg as taught by Endoh.

The motivation for doing so would have been to increase durability by ensuring that the layers the adhesive holds together does not separate (Endoh, column 2 lines 1-19).

4. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Booth and Tsukamoto as applied to claims 1-3, 5, 8-10 and 12 above, and further in view of **Kikuchi et al (US 2003/0128907 A1)** (Kikuchi).

The combination of Booth and Tsukamoto teaches the integrated circuit with the limitation described above used to reject claims1-3, 5, 8-10 and 12 above.

The combination of Booth and Tsukamoto does not teach expressly a stepped portion near two via holes with a waveguide attached.

Kikuchi teaches a method of manufacturing an opto-electric wiring board comprising via hole (Fig. 3I, 74) contacts and an optical fiber (82) attached to a stepped portion of wiring board (7).

The combination of Booth and Tsukamoto and Kikuchi are analogous art because they are from the same field of endeavor, processes to create integrated circuit and via holes.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to attach a waveguide at taught by the combination of Booth and Tsukamoto or to a stepped portion as taught by Kikuchi. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a waveguide inside the board structure or attached externally to a stepped portion, both will transmit a light signal.

The motivation for doing so would have been to increase efficiency by reducing distortion and transmission loss of the optical signal (Kikuch, paragraph 0007).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- The following references teach electrical via holes made in similar processes to the applicant's: Uematsu et al (Us 6,787,710 B2), Dux et al (US 5,224,265), Ehrenberg et al (US 5,232,548), Suppelsa et al (US 5,421,083), Gates, Jr. et al (US 5,568,682), Bhatt et al (US 5,707,893) & (US 6,195,883 B1), Kobayashi et al (US 2001/0010250 A1), Yamamoto et al (Us 2003/0129383 A1).
- Asai (US 2004/0212030 A1) teaches electric and opto via holes made in similar processes to the applicant's.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Lepisto whose telephone number is (571) 272-1946. The examiner can normally be reached on M-F 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RAL

Ryan Lepisto

Art Unit 2883

Date: 12/2/04

Frank Font

Frank Font

Supervisory Patent Examiner

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